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## **SRC Selects Altera for Next Generation MAP Processor**

### *Further Collaboration Provides Floating Point Compiler for SRC Systems*

**San Jose, Calif., November 12, 2007**—Altera Corporation (NASDAQ: ALTR) today announced that SRC Computers, Inc. has chosen the Stratix<sup>®</sup> II FPGA device for their new Series I MAP reconfigurable processor module used in high-performance computing applications such as financial, defense, energy and biometrics. Systems built with the Series I MAP are part of the SRC-7 product line that can accelerate applications such as Black-Scholes or medical imaging by over 30 times compared to current dual-core CPUs.

The Series I MAP is a high-performance compute processor module used to off load the system processor of compute-intensive applications. It uses the system memory bus to communicate to and from the system processor. The memory bus interface is a cost-effective, low-latency, high-throughput interface ideal for fast data transfer to and from the system processor. The Series I MAP processor plugs into a computer memory slot providing the user with a high-performance, direct-execution logic processor providing millions of gates of user logic, autonomous control functions to minimize overhead effects, high on-board memory bandwidth and high-speed interconnects to the system as well as other MAPs.

“We’ve worked closely with SRC, supplying them with both a silicon solution as well as a technology solution,” said Misha Burich, senior vice president of engineering at Altera. “By adding the acceleration capabilities and the computing power of Stratix II FPGAs to SRC’s high-performance computing solutions, these targeted, double-precision FP applications are attaining incredible performance gains, while realizing a dramatic decrease in system power consumption and cost.”

Altera is further collaborating with SRC by providing them with a floating point (FP) compiler enabling accelerated performance and higher logic utilization for their SRC-7 product line. The entire SRC-7 product line maximizes performance by using Altera<sup>®</sup> Stratix II FPGAs. The collaboration provides SRC with a FP compiler for their high-performance systems. For

those applications with FP data types, performance can be increased by up to 33 percent compared to existing place and route tools. Using the FP compiler, results in more efficient routing with up to 50 percent less logic required and significant power savings from the logic reduction. The FP compiler enables a Stratix II FPGA to deliver in excess of 20 sustained double precision GFLOPS for fast Fourier transform (FFT) or matrix math applications.

“Our testing and analysis shows that Altera FPGAs provide the highest computational performance available with an additional overall improvement of 5 to 10 GFLOPS when used in conjunction with their FP compiler in our MAP processor modules,” said Jon Huppenthal, CEO of SRC. “This further enhances the FLOP/watt ratio that FPGAs can deliver over other alternatives, making them extremely cost-effective for high-performance computing solutions.”

The Altera FP compiler is being distributed first as part of SRC’s Carte high-level language programming environment and is currently under evaluation by other tool chain suppliers.

### **About Altera**

Altera programmable solutions enable system and semiconductor companies to rapidly and cost-effectively innovate, differentiate and win in their markets. Find out more at [www.altera.com](http://www.altera.com).

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