

SRC-7 Performance and Resource Management Workshop

A three-day workshop on SRC-7 Performance and Resource Management is available at SRC Computers' headquarters in Colorado Springs, Colorado. Participants may also elect to return for ½ day after the workshop to work on their code and have additional questions answered by the instructors. There is no additional charge for this ½ day session.

Workshops are typically held Tuesday through Thursday with the optional ½ day held on Friday morning. The workshop begins at 8:30 a.m. the first day.

Agenda

Lesson 1: Debug and Execution Environment

Lesson 2: DMAs and Computational Improvements

Lesson 3: Loop Slowdowns

Lesson 4: Using Block RAM Arrays

Lesson 5: Studying Loop Carried Scalar Dependencies

Lesson 6: Loop Nest Optimizations

Lesson 7: Converting an Example to 32-bit Mode

Lesson 8: Creating User Macros for the MAP[®] Compiler

Lesson 9: Stateful Macros

Lesson 10: External Macros

Lesson 11: Examining Pure Periodic Functions

Lesson 12: Writing a Routine Using Parallel Code Sections

Lesson 13: Writing a Routine Using Streams

Lesson 14: Writing a Simple Routine that Uses Two FPGAs

Lesson 15: Writing a Routine Using Inlining of Subroutines

Lesson 16: Using Floating Point

Lesson 17: Using a Delay Macro to Perform a Stencil Computation with Minimal Memory Traffic

Lesson 18: Using Common Memory

Lesson 19: Using Barriers and MAP Processors

Lesson 20: Using MAP GPIO Ports

Lesson 21: Using Barriers on MAP and Microprocessor

Optional ½ Day - User Code Example

For workshop pricing or to check future schedules please contact:

Mark Tellez, Director of Business Development

Phone: (719) 262-0213 x173, Fax: (719) 262-0223

Email: mtellez@srccomputers.com