

Series H MAP® Processor

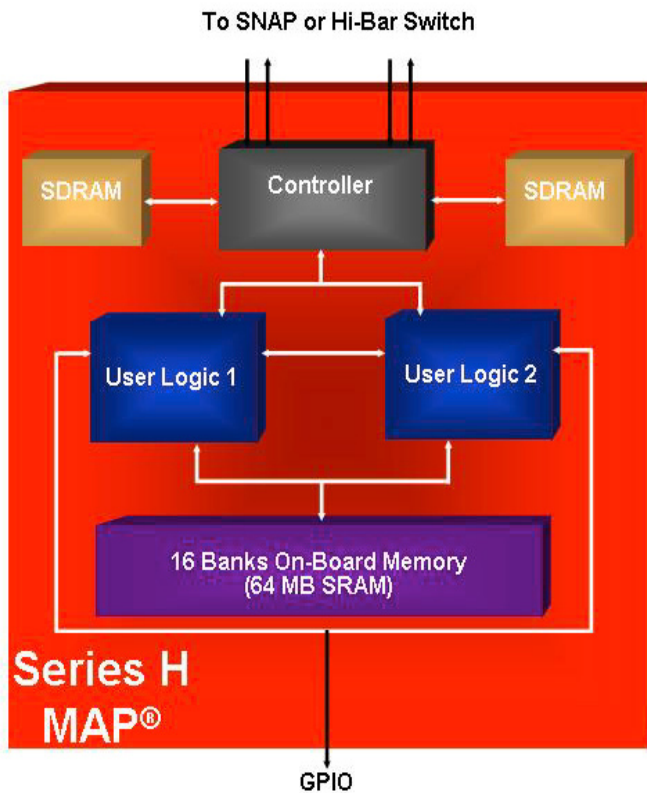
The patented MAP® processor is the SRC® high performance explicit processor. This reconfigurable processor typically achieves orders of magnitude increases in performance as compared to standard microprocessors. The end result is an increase in compute density that allows any computer built with a MAP processor to be made orders of magnitude smaller than with microprocessors.

The MAP processor uses reconfigurable components to accomplish both control and user-defined compute, data prefetch and data access functions. This compute capability is teamed with very high on and off-board interconnect bandwidth. The MAP processor's multiple banks of On-Board SRAM Memory provide very high local memory bandwidth. MAP modules are equipped with separate input and output ports with each port sustaining multiple gigabytes of data payload bandwidth resulting in multiple times the sustained bandwidth of a typical PCI Express interconnect on each port. Each MAP module also has two General Purpose I/O ports for direct MAP module-to-MAP module connections or direct sensor data input.



Series H MAP Processor

- H - 1.75 in. (4.44 cm) - Air cooled
- W - 5.85 in. (14.86 cm) - Air cooled
- D - 8.00 in. (20.32 cm) - Air cooled



Individual MAP processors are housed in a 5.25-inch drive bay enclosure along with the cooling solution and power converters. Each MAP processor is powered by +12v from a standard disk drive connector. This form factor allows the easy incorporation of MAP modules into commodity enclosures for MAPstation™ Workstations.

Series H MAP® Specifications

	MAP Processor Series
	H
Logic	
User Logic Chips	EP2S180
Control Logic Chip	EP2S130
Nominal Clock Rate (MHz)	150
Total User Logic Reconfiguration Time (ms)	100
On- Board-Memory (OBM)	
# On-Board-Memory Banks - Logical	16
# On-Board-Memory Banks - Physical	8
Total OBM Bandwidth (BW) (Gbytes/s)	19.2
OBM BW to User Logic (Gbytes/s)	19.2
OBM BW to Control Logic (Gbytes/s)	7.2
OBM Bank Width (bits)	64
Total Simultaneous OBM Accesses (reads or writes)	16
Simultaneous User Logic OBM Accesses (reads or writes)	16
Total OBM Size (Mbytes)	64
Bridge Port BW (Gbytes/s)	4.8
MAP processor to System Interconnect	
Sustained MAP Input Payload BW from System (Gbytes/s)	7.2
Sustained MAP Output Payload BW to System (Gbytes/s)	7.2
Simultaneous Sustained MAP Payload I/O BW to and from System (Gbytes/s)	14.4
General Purpose I/O (GPIO)	
Number of GPIO Ports per MAP	2
GPIO Signal Level Standards	2.5VTTL/ LVDS
# Signal Paths per GPIO Port	96/48
Sustainable GPIO BW per Port (Gbytes/s)	3.6/4.8
Maximum Data Rate per Signal Path (Mbits/s)	300/1000
GPIO Interconnect Medium	User Determined
Physical Specifications	
Power Supply Voltage	+12vdc
Maximum Power Consumption (watts)	80
Form Factor	5.25
Cooling Methodology	Air
MTBF (Khours)	195
Availability	Now

Series C, D, E, F, and G MAPs are no longer available.

SRC Computers reserves the right to change these specifications at any time.